

AMENDMENT

In the Specification:

Please replace paragraph 0017 with the following paragraph:

[0017] The numerous advantages of the present invention may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. 1 illustrates a fluted pin of a first embodiment;

FIG. 2 illustrates a fluted pin of a second embodiment with a hemispherical pin cap;

FIG. 3 illustrates an array of fluted pins mounted in a support membrane in a perspective view;

FIG. 4 illustrates a cross section of an array of fluted pins mounted in a support membrane;

FIG. 5 illustrates a four pin support stanchion;

FIG. 6 illustrates a three pin support stanchion;

FIG. 7 illustrates four three pin support stanchions placed on a circuit board or substrate;

FIG. 8 illustrates a seven pin enclosed stanchion;

FIGs. 9A, 9B, and 9C illustrate cylindrical pins;

FIGs. 9D and 9E illustrate a fluted pin; and

FIGs. 10A, 10B, and 10C illustrate cross sections of three variations of fluted pins;

FIG. 11 illustrates a cutaway view of a circuit structure with membrane of the present invention;

FIG. 12 illustrates a cutaway view of a circuit structure with stanchions of the present invention;

FIG. 13 illustrates a signal pin with a screwed on cap of the present invention; and

FIG. 14 illustrates an embodiment in which the support member entirely encloses an area of unattached signal pins.

Please replace paragraph [0026] with the following paragraph:

B2 [0026] FIG. 2 illustrates a fluted pin of a second embodiment with a hemispherical pin cap (HPC) 40 and a triangular cross section 30. Cross sections such as oval, circular, square, polygonal, and other shapes may alternatively be employed. The HPC 40 pin cap may have a maximum height approximately equal to 1/3 the diameter of a sphere based on a standardized solder ball used on BGA packages. The HPC 40 may be made of a material having a relative dielectric constant ϵ_r as close to 1 as possible. It may also have be made of a high dielectric constant material. The material should have a high melt temperature. It also should have a deformation coefficient to allow the fluted pin to be inserted through it or to be molded onto or around the fluted pin. The HPC material, in another embodiment, may be metallic. For example, it may be made from solder ball materials. The HPC may be formed around the pin or have a hole through the radial axis through which the pin could be inserted in a displacement fit. For instance, it could be screwed onto the end of the signal pin 10, as illustrated in FIG. 13. In FIG. 13, the HPC screws (via screw 150) into a hole 140 of the signal pin 10.

Please replace paragraph [0030] with the following paragraph:

B3 [0030] As shown in FIGs. 3 and 4, a first supporting structure is a membrane 50 to hold signal pins in a precise array that will allow an automated or manual attachment of signal pins to BGA or PBGA (pin ball grid array) packages. The supporting structure holds signal pins for mass production attachment to BGA and PBGA packages 120 without interacting with signal transmission parameter and degrading them, as shown in FIG. 11. In FIG. 11, recesses 125 on the underside of the integrated circuit package 120 facilitate attachment of the HPC 40 of signal pin 10. The signal pins 10 electrically connect the integrated circuit package 120 with a circuit board 130. The membrane allows high volume attachment production of signal pins onto either BGA or PBGA type packages. The membrane allows automated signal pin replacement with automated repair equipment.

Please replace paragraphs [0035] to [0042] with the following single paragraph:

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- [0035] As shown in FIGs 5-8, 12, and 14, a second supporting structure is a multipin stanchion. In a multipin stanchion, a cylindrical braced pin array allows the construction of PBGA packaging with wired signal pins for signal conduction and connection between BGA/ chip substrate and circuit board. The stanchion holds wire signal pins in a vertical and horizontal stable position for mass production attachment of PBGA packages to circuit board. A minimum of three cylinders are attached together to form at a minimum one right angle pin array. The cylinders and the interconnecting braces are of sufficient material thickness to provide a rigid structure that when placed between a PBGA (pin ball grid array) substrate and the PCB will hold the PBGA in a stable position during the pin attach solder process for PBGA to PCB lands. FIG. 5 shows a four pin support stanchion 80. The stanchion may be an array of side by side pins or span one or more pad lands. Pin supports 70 are formed at right angle intersections of support walls 60. FIG. 6 illustrates a three pin support stanchion 80. In normal practice, four of a like kind array, either 3 or 4 position, may be placed at equal distance points on a PBGA to maintain its vertical stability during attachment to a PCB. Two would be the minimum needed for a 3 pin stanchion. One for 4 or more pin stanchions. A two pin stanchion may be used in certain applications. Many other materials may be used for the PCB beside FR4, such as flex circuit kapton. Surface mount devices (SMD) and through hole (TH) components may be attached with high temperature solder reflow processes or with electrically conductive adhesives. FIG. 7 illustrates four three pin support stanchions 80 placed on a circuit board or substrate 55. The stanchions 80 are placed at the corners of the location where the integrated circuit package will be set down. The bottom ends of the pins are placed on the circuit board pads that normally receive the solder balls of a BGA/ chip package. Interior pins may be placed free of any stanchion or other support. FIG. 8 illustrates a seven pin enclosed stanchion. This would form the resting place for an integrated circuit package. FIG. 12 shows a cutaway view of a BGA/ chip package 120 having recesses 125 that receive the HPC 40 of a signal pin 12, 14 that electrically connects to a circuit board 130. In FIG. 12, a portion of the signal pins 12 are supported by stanchions 80 and a portion of the signal pins 14 are unsupported. FIG. 14 shows an array of signal pins 12, 14, in which a stanchion 80 entirely encloses an area of unsupported signal pins 14.